Medipix2, a 64k pixel read out chip with 55 mm square elements working in single photon counting mode[1]

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***Abstract*-- The *Medipix2* chip is a pixel detector readout chip consisting of 256 x 256 identical elements, each working in single photon counting mode for positive or negative input charge signals. Each pixel cell contains around 500 transistors and occupies a total surface area of 55 mm x 55 mm. A 20 mm width octagonal opening connects the detector and the preamplifier input via bump-bonding. The preamplifier feedback provides compensation for detector leakage current on a pixel by pixel basis. Two identical pulse height discriminators are used to create a pulse if the preamplifier output falls within a defined energy window. These digital pulses are then counted with a 13-bit pseudo-random counter. The counter logic, based in a shift register, also behaves as the input/output register for the pixel. Each cell also has an 8-bit configuration register which allows masking, test-enabling and 3-bit individual threshold adjust for each discriminator. The chip can be configured in serial mode and read out either serially or in parallel. The chip is designed and manufactured in a 6-metal 0.25 mm CMOS technology. Preliminary measurements show very good agreement with simulations.**

I. INTRODUCTION

ADVANCES in CMOS technology open up new possibilities in particle detection and imaging. In recent years particle physics experiments have been transformed by the introduction on ASIC circuits particularly for tracking detectors. Pixel detectors have become key components in tracking systems especially in high multiplicity environments where excellent spatial resolution is combined with extremely high signal to noise ratios allowing physicists to find traces of rare particle tracks in very complicated events [1]. At the same time investigations have been continuing into the adaptation of this technology to X-ray imaging applications. In particular this technology enables the counting of particles which are deposited in each pixel. A first large prototype chip, the Photon Counting Chip (PCC or Medipix1) [2], has been successfully developed and measured. This chip demonstrated that the photon counting approach provides images with excellent dynamic range which are practically free of non-photonic noise [3]. The performance of the system was limited mainly by the size of the pixel (170 μm x 170 μm) which was determined by the component density of the 1 μm CMOS process used.

Encouraged by these results we decided to make a new version of the chip in a 0.25 μm CMOS technology. Each pixel measures only 55 μm by 55 μm and contains around 500 transistors. This reduction in pixel dimension is possible because of the tiny dimensions of the individual transistors as well as the high number of metal interconnect layers. The new system provides a spatial resolution comparable to that achieved by much simpler integrating read out systems whilst keeping excellent signal-to-noise and dynamic range, inherent properties of the photon counting method. Moreover, some new features could be included in the pixel cell: leakage current compensation on a pixel by pixel basis, sensitivity to carriers of both types and an energy windowed discriminator.

The architecture and functional behavior of Medipix2 chip are described in this paper. First preliminary measurements are presented. Some new ideas for future pixel detectors are explained at the end of this paper.

II. CHIP DESCRIPTION

The Medipix2 chip has been designed to minimize the dead area between chips covering large areas when butting several chips together. This is achieved placing the *periphery* at the bottom of the chip, and minimizing the *non-sensitive area* in the other three edges to less than 50 μm. Figure 1 shows the *Medipix2* floor plan organization. The *sensitive area* (top box) is arranged as a matrix of 256 x 256 pixels of 55 x 55μm^2 resulting in a detection area of 1.98 cm^2 which represents 87% of the entire chip area. The periphery (bottom box) contains 13 8-bit DACs and the Input/Output control logic. There are 5 lateral IO wire-bonding pads which can be used to make a daisy chain of chips. In a multi-chip detector there would be no dead area between neighbouring chips, but the edge

[1] This project has been undertaken in the framework of the Medipix2 Collaboration. http://www.cern.ch/MEDIPIX

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columns of each chip are connected to sensors which are 165 µm wide.

Both the analog and digital circuitry have been designed to operate with independent 2.2 V power supplies with a total analog power consumption of about 500 mW. The chip contains around 33 million transistors.

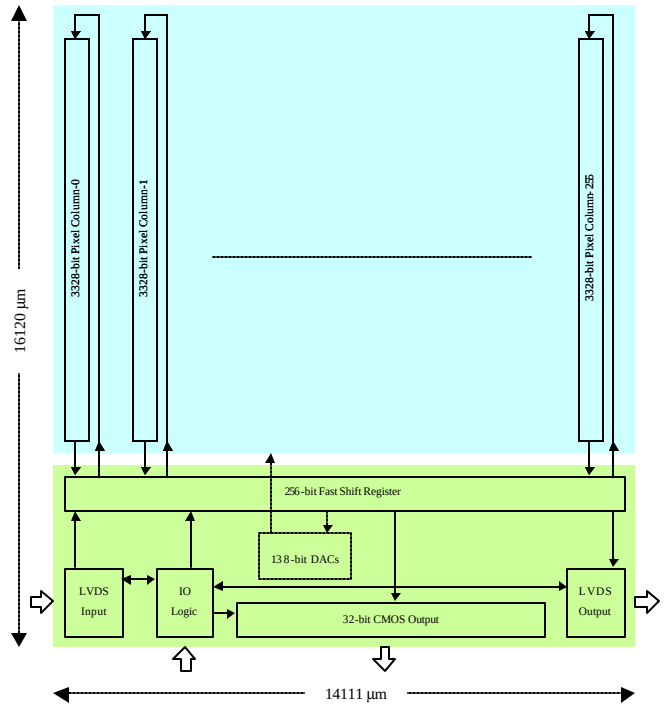

Figure 1: Schematic floorplan of the Medipix2 chip.

A. *The Pixel Cell*

Charged particles interacting in the detector material deposit a charge which drifts towards the collection electrodes under the influence of the detector bias voltage. This charge is then amplified and compared with two different thresholds that form an energy window. If the detected charge falls inside this energy window the digital counter is incremented.

Each pixel has eight independent configuration bits. Six of them are used for the fine threshold adjustment (three bits for each discriminator), one for masking noisy pixels, and one to enable the input charge test through the 8 fF on-pixel capacitance.

Figure 2 shows the schematic and the layout of the Medipix2 pixel cell. The analog side (left box) contains a charge preamplifier with DC leakage current compensation, a test capacitance, and two branches of identical discriminators. The digital side (right box) contains the Double Discriminator Logic (DDL) and the 13-bit shift register.

The dimensions of the cell are 55 x 55 µm^2. Each pixel has 504 transistors and a static power consumption of ~8 µW. The octagonal bump bond opening, placed on top of the analog side, has a diameter of 20 µm.

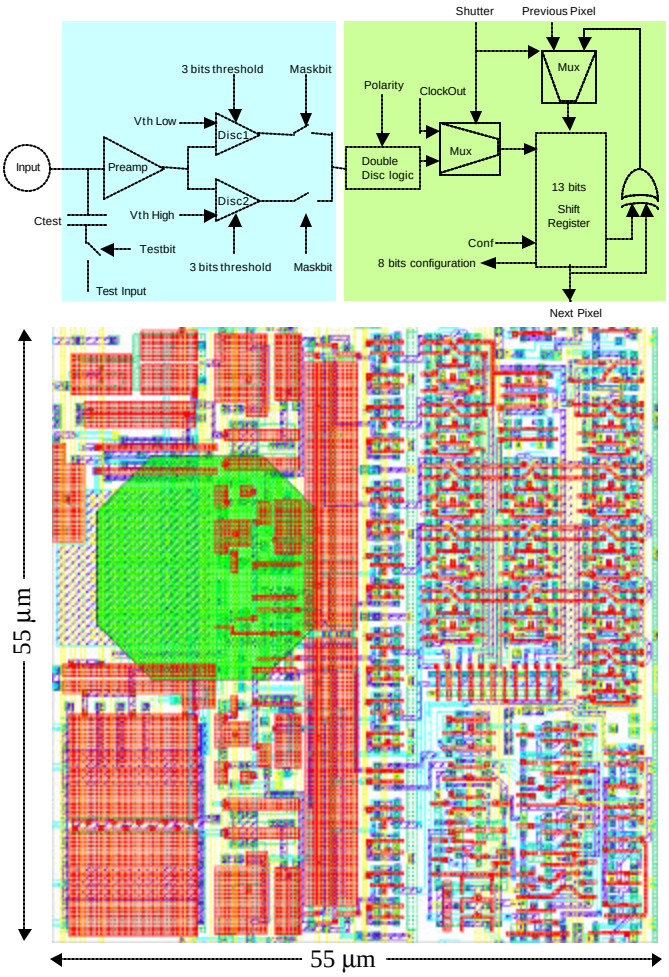

Figure 2: Medipix2 pixel cell schematics and layout.

1) *The charge Preamplifier*

The preamplifier follows the scheme proposed by Krummenacher [5] based on a differential CMOS amplifier as shown in Figure 3. A differential input amplifier was chosen for better rejection of substrate and power supply noises.

This configuration provides a constant current fast return to zero through the transistors M1a and M1b controlled by the I_{Krum} current DAC. The M2 transistor compensates the detector DC leakage current. Positive leakage currents (hole collection) smaller than I_{Krum} and negative (electron collection) smaller than $I_{Krum/2}$ can be compensated in each pixel. Another voltage DAC controls the V_{fbk} node. This node sets the DC output voltage optimizing the dynamic range depending on whether holes or electrons are being collected. The polarity of collection is selected using the *Polarity* input pad at the DAC level. The change of this voltage affects the overall gain of the preamplifier due to the change in the biasing point, resulting in slightly different gains for the two collection modes.

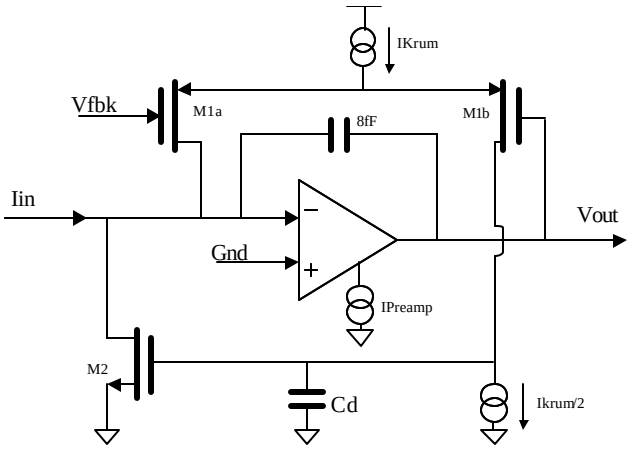

Figure 3: Preamplifier scheme.

2) The Discriminator

The output of the preamplifier feeds two identical discriminators which are linear over a wide range. These two branches are independent and the discrimination energy can be set differently depending on the application. The difference between the two energy levels ($W_{th}=V_{thHigh}-V_{thLow}$), defines the energy window (W_{th}) into which the incoming particle energy has to fall in order to increment the counter. This window discrimination is performed by the DDL (*Double Discrimination Logic*).

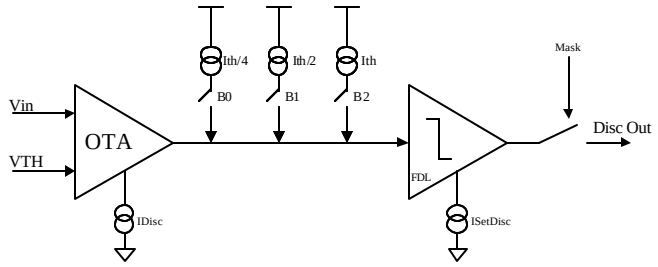

Figure 4: Discriminator scheme

If the V_{thHigh} is set to be smaller than V_{thLow}, the DDL works in single discrimination mode, and the counter is incremented when the incoming particle energy exceeds the V_{thLow} threshold.

In Figure 4 only one discriminator branch is shown. Each branch includes a differential amplifier configured to work as an OTA (*Operational Transimpedance Amplifier*), three independent selectable current sources to minimize the spread of the threshold distribution from pixel to pixel, and a current discriminator. The output can be masked in case of malfunction or excessive noise.

3) The Shift Register

The shift register has two modes depending on the state of the *Shutter* signal. When the *Shutter* is low the shift register works as a pseudo-random counter of 13 bits with a dynamic range of 8001 counts. Every pulse coming from the discriminator logic increments by one the counter value. When the *Shutter* is high an external clock can be used to shift the data from pixel to pixel. This mode is used both for setting the 8 configuration bits and for reading the 13-bit counter information.

B. The Periphery

The periphery contains;

- 13 8-bit DACs [6] which set the different bias voltages in the chip;
- A 256-bit FSR (*Fast Shift Register*) for configuration or readout;
- 127 Input/Output pads;
- LVDS drivers and receivers;
- IO logic that controls the chip.

When the matrix is accessed to perform any IO operation the data is organized in 256 columns of 256x13 bits. Therefore each chip has 851968 bits to be read or written for any matrix IO operation. The *Medipix2* uses a high-speed *LVDS* (*Low Voltage Differential Signaling*, [7]) logic for configuration and readout of the chip in serial mode. Also a parallel 32-bit single-ended CMOS bus is present for applications requiring even higher readout frame rates. The setting of the configuration register in the entire matrix and of the 13 8-bit DACs is done serially through the LVDS receivers. Using a clock of 100 MHz the entire matrix is read out in less than 9 ms through the serial port, while using the parallel option the readout would take 266 μs using the same clock frequency.

III. MEASUREMENTS

Preliminary measurements were performed using an *IMS ATS* digital IC tester. All of the logic at the chip periphery (see Figure 1) functioned at 100 MHz, which is the highest clocking frequency available on the IC tester. The setting of the DACs, the Fast Shift Register, the peripheral control logic, the 32-bit CMOS bus and the *LVDS* drivers and receivers performed as in simulations.

First characterization of the pixel front-end has been achieved by applying a test pulse to the on-pixel injection capacitance of several pixels. Output pads from a 3x3 pixel cluster of the active matrix have been provided and these allow direct access to the preamplifier outputs. There is also a pad which outputs the OR of the 9-discriminator outputs. An example of these test outputs is seen in Figure 5. These output pads along with the pixel counter information enable the pixel cell to be characterized. Table 1 summarizes these measurements. All the sub-blocks of the pixel cell perform as in simulation.

The electronic noise is measured using the s-curve method. Having a fixed threshold a number of input charge pulses are applied via the injection capacitance. This charge is gradually increased while the counter contents are monitored. The counter contents as a proportion of the number of applied pulses is plotted versus the amplitude of the injected charge creating an s-shaped curve. The effective threshold is at 50%

of this s-curve. The charge difference between the 97.75% and 2.25% of the s-curve is four times the RMS noise of the front-end assuming gaussian distributed noise. Having a double discriminator system, the electronic noise for each branch can be estimated. The first is generated when the injected charge crosses the V_{thLow} threshold (s_{nL}), and the second when crossing the V_{thHigh} threshold (s_{nH}). The threshold dispersion in one row is also shown for both threshold crossings (s_{nTHL}, s_{nTHH}). The threshold dispersion between pixels can be later corrected adjusting the 3-bit threshold fine-tuning present in each discriminator branch. For deposited charges smaller than 50 ke^- a maximum count rate of 1 MHz per pixel is obtained without pile-up following the specifications.

TABLE 1: PREAMPLIFIER MEASURED CHARACTERISTICS

	Electron Collection	Holes Collection
Gain	*12.5 mV/ke⁻*	*13.25 mV/ke*
Non linearity	*<3% to 100 ke⁻*	*<3% to 80 ke⁻*
Peaking time	*<150ns*	
Return to baseline	*<1ms for Qin <50 ke⁻*	
Electronic Noise	*s_{nL}~ 141 e⁻ s_{nH}~ 200 e⁻*	
Threshold dispersion in 1 row	*s_{nTHL}~ 360 e⁻ s_{nTHH}~ 800 e⁻*	
Analog power dissipation	*~8 mW/channel for 2.2V supply*	

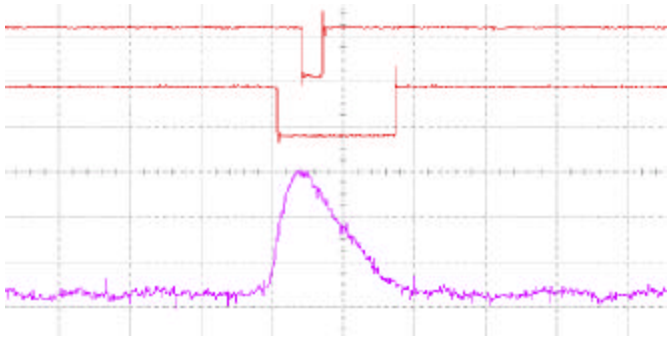

Figure 5. Preamplifier analog output response to an injected charge of 17200e^-, and discriminator digital output with threshold setting at 16400e^- (top) and 6300e^- (bottom). X=500ns, Y_{analog}=50mV, $Y_{digital}$=2V.

A radiation hardness measurement of *Medipix2* has been made using a dedicated machine (*Seifert RP149*). The target material used in the tube was tungsten and the X-ray energy peaked at 10 keV. Doses of 3.9 krad/min up to 150 krad and 8.04 krad/min from 150 krad to 500 krad were applied to the chip. An increase of the analog power supply current was observed from 200 mA to 260 mA, while a knee at around 200 krad was observed in the digital power supply, which feeds more than the 90% of the chip transistors. After an irradiation of 500 krad the chip was annealed (1 week at 100°C) and it recovered to pre irradiated values.

IV. FUTURE DEVELOPMENTS

As pixel dimensions shrink with CMOS scaling *charge sharing* becomes an important issue in photon counting pixel systems [8]. The size of the charge cloud generated by a photon in the detector material depends on the energy of the incoming photon, the mobility of the material and the collection time of the carrier. The study of energy deposition in segmented sensors and the signal formation in pixel detectors with different geometries will be the subject of numerous future studies.

At this point a short description of some aspects can be given already. We describe two different approaches to deal with the effects of *charge sharing*, one at the detector level and the other one at the electronics level.

A. *Proposed detector solution*

In a square pixel matrix the distance between a pixel and its orthogonal neighbors is shorter than to the diagonal neighbors. Using hexagonal pixels, as shown in

Figure 6, one can create a homogeneous environment for each pixel, with six equal neighbors. By doing this, the distance between neighboring pixels is constant in all directions achieving a much better spatial uniformity than with square pixels.

This homogeneity in the sensor can only be achieved at the cost of more complexity in the readout. In order to physically match the hexagonal detector with the electronics, the pixel cells at the electronics level must be rectangular, as shown in

Figure 6. Moreover, from column to column they have to be shifted up or down by half a cell.

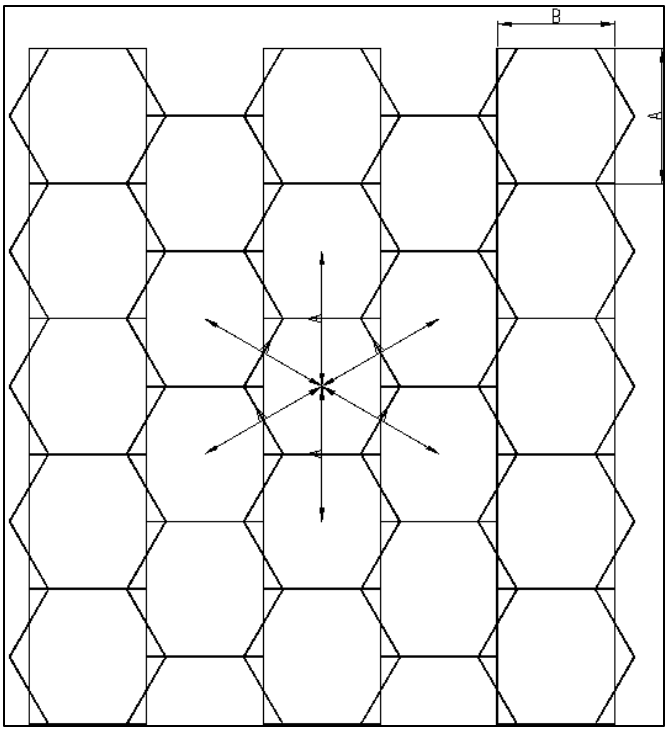

Figure 6: Proposed detector layout. B=3A/2v3

B. *Proposed electronic solution*

In order to avoid either missing or double counting photons which share charge between pixels it is necessary to sum pulses over local pixel clusters. The sum should be compared with one or more energy thresholds and the hit (and energy) accorded to the pixel with the greatest energy deposit. Ultimately one could aim to have a multi channel analyzer logic in one pixel. We suggest here one possible implementation of such a system.

Assuming that the *charge sharing* effect only happens between adjacent pixels, a charge sharing control system can be built using the information coming from the 6 surrounding pixels and comparing it with the central pixel creating a 7-pixel cluster cell, as shown in Figure 6.

In the proposed scheme of Figure 7 the discriminator output pulse (*DiscOut*) from each pixel is sent to its 6 neighbors. A voltage level discriminator generates this pulse with a threshold level set to a fixed value in the entire pixel matrix, probably slightly higher than the amplifier electronic noise (typically >3 times). The discriminator output pulse length is proportional to the charge deposited in the pixel. Two items of useful information can be obtained from the local pulse and the six neighboring pixels pulses. First, if the local pulse length is longer than any of the other six neighboring pixel pulses, then the local pixel collected the biggest *share* of charge generated by the incoming particle. This gives information of the position where the particle converted with an error smaller than $2A/\sqrt{3}$ with respect to the pixel centroid (where A is the apothem of the hexagonal pixel). Second, adding up all the discriminator pulses (or the amplitudes at the preamplifier outputs), one can get the total deposited charge in this 7-pixel cluster. This can be compared with a global threshold level (*Global Threshold Level2*) or window in order to count only the photons with energies higher than the fixed threshold or falling within the window. These two last conditions must then be asserted at the same time to increment the counter. Obviously the scheme could be extended to a multi window system.

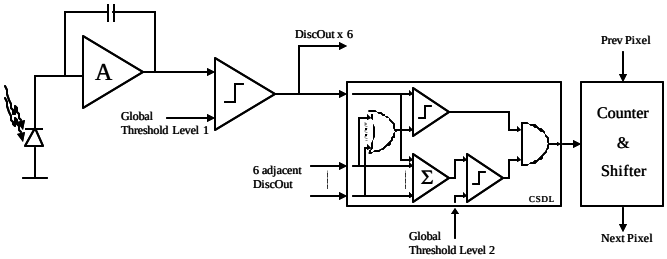

Figure 7: Scheme of the proposed solution to take into account charge sharing effects.

This proposed system has to face two major constraints. Firstly, the design and layout of a cell with inter-pixel connections which must be contained in a very small area is very difficult to achieve with our present design technology (0.25 μm minimum gate length and 6 metal layers). This can be overcome by moving to more advanced CMOS technologies with smaller gate length and more interconnection metal layers. The second constraint is the design of very low noise amplifier and discriminator cells, in order to minimize the threshold spread and mismatch between adjacent channels.

The functionality of the system described could also be achieved using ADC's per pixel and adding ADC values. However, the proposed implementation has the advantage of simplicity.

V. Conclusions

A 64k channel pixel detector readout chip has been designed and fabricated using a deep sub-micron CMOS technology. It has been possible to implement a full pulse counting readout system in a pixel cell of only 55 μm x 55 μm. Preliminary test results showed very good agreement with simulations.

New ideas for dealing with charge sharing in future photon counting devices have also been presented.

VI. Acknowledgment

The authors would like to thank all members of the *Medipix Collaboration* for their support and encouragement.

VII. References

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