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An introduction to deep submicron CMOS for vertex applications

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Abstract

Microelectronics has become a key enabling technology in the development of tracking detectors for High Energy Physics. Deep submicron CMOS is likely to be extensively used in all future tracking systems. Radiation tolerance in the Mrad region has been achieved and complete readout chips comprising many millions of transistors now exist. The choice of technology is dictated by market forces but the adoption of deep submicron CMOS for tracking applications still poses some challenges. The techniques used are reviewed and some of the future challenges are discussed. © 2001 Published by Elsevier Science B.V.

Keywords: CMOS; Readout electronics; Vertex detectors

1. Introduction

The development of readout electronics for the vertex detectors of the future LHC detectors is progressing rapidly. Custom designed ASICs have become crucial components of these systems and microelectronics is now recognised as a key enabling technology in experimental High Energy Physics (HEP). This activity runs concurrently with the continuous shrinking of gate lengths in commercial CMOS processes. This paper discusses briefly the motivations for this trend in commercial CMOS and explores the implications of the trend for vertex detector readout electronics. Radiation hardness is an important issue for these applications. Radiation effects in deep sub-micron CMOS are reviewed briefly. Special layout and circuit topologies can be used to design radiation tolerant readout chips. The techniques used are discussed. Moreover, CMOS component density is a critical parameter in determining the cell size of pixel detectors which form the inner layers of most of the trackers. It will be shown that sufficiently small pixel sizes (50–100 μm) can still be achieved in spite of the area penalty incurred in using radiation tolerant design techniques. Some of the implications of future device scaling will be discussed. This will force designers to rethink circuit topologies which are suitable to the much reduced power supplies of the future very deep sub-micron processes.

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2. Trends in CMOS electronics

Each year the Semiconductor Industry Association (SIA) produces a Roadmap[2] which predicts the evolution in the industry over the following 15 years. In the 1999 edition of the Roadmap [1], gate lengths are predicted to fall from the present day 180 nm to 35 nm by 2014 accompanied by a fall in power supply from the present 1.8 V to 0.6 V. The shrinking of the transistor dimensions enables an exponential increase in component density with time. This increase in component density combined with the constant cost per unit area of silicon explains the motivation of the industry to continue along the same arduous path. A refusal to adopt the latest technology is inevitably accompanied with loss of market share as competitors are able to provide the same chips cheaper or more advanced chips at the same price. The mobile telephone market provides clear testimony. The HEP community will be obliged to follow this trend in technology. Moreover, a modern CMOS facility with a typical capacity of several hundred thousand wafers per year involves investments of around $2 billion. One can appreciate that special processes may not be maintained for a low volume, low cost niche market.

3. Radiation effects in CMOS

As the inner layers of the LHC experiments are to operate in a highly irradiated environment with total doses in the Mrad range radiation effects are a key issue for the design. Fortunately, solutions have been identified over the last few years to avoid serious degradation of performance, even up to 30–50 Mrad [2]. Radiation effects are divided into roughly two categories: total dose effects and single event effects. Total dose effects in CMOS are mainly associated with charging of the oxides. An excellent summary of these effects is provided in Ref. [3]. During irradiation, electrons and holes are generated in the oxides. While the electrons are evacuated within ns, holes accumulate in traps leading to transistor threshold voltage shifts. As the oxides get thinner, the charging decreases in proportion to the volume of the oxide. This provides an improvement in transistor threshold voltage shift which is roughly proportional to the inverse of the square of the oxide thickness. Hence, thinner oxides are inherently more radiation hard. Moreover, as the oxide thickness falls below 10 nm, the decrease in the radiation induced threshold voltage becomes even more pronounced as illustrated in Fig. 1 [4]. This is thought to be a result of electrons which tunnel into the oxide recombining with the radiation induced trapped holes. Therefore, for deep sub-micron processes (a 0.25 μm process has a gate oxide thickness of ≈5 nm) radiation induced threshold voltage shift becomes negligible even at very high doses. However, there are still possible leakage paths from drain to source and from one transistor to another which have to be eliminated by special layout techniques. These are described in detail in Ref. [5]. In general, NMOS transistors should be

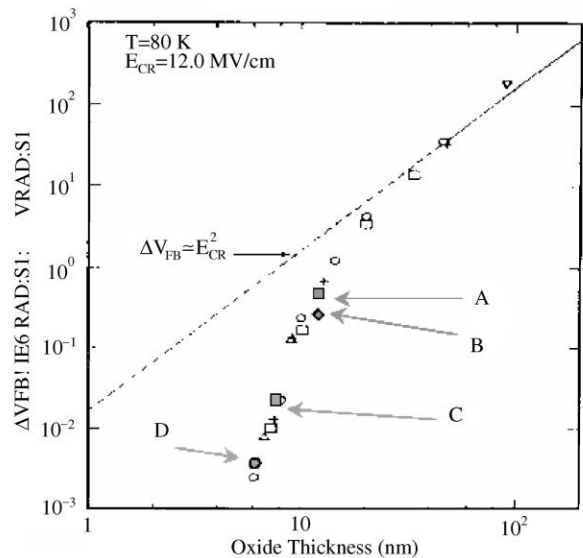

Fig. 1. Flatband voltage shift of MOS capacitors at different gate oxide thicknesses for 1 Mrad (SiO_2) irradiation taken from Ref. [4]. The square points are threshold voltage shifts measured on transistors from different CMOS processes.

[2] The document is sponsored by the Semiconductor Industry Association (SIA), the European Electronic Component association (EECA), the Electronic Industries Association of Japan (EIAJ), the Korean Semiconductor Industry Association and Taiwan Semiconductor Industry Association.

drawn with closed gates eliminating leakage paths from drain to source and neighbouring n^+ implantations should be separated by p^+ guard rings. The implications for the design of electronics will be discussed later.

Single event effects may also be an issue in the LHC inner tracker systems. These are discussed here in order of gravity.

Single event gate rupture (SEGR) is a catastrophic breakdown of a transistor gate which occurs when a highly ionising particle induces an avalanche breakdown of the gate oxide. Fortunately, the effect only manifests itself above a critical threshold electric field and this critical field has been observed to increase with reduced gate oxide thickness. Fig. 2, taken from Ref. [6], illustrates this. Also indicated is the maximum field which is permitted in a 0.25 μm process on a 5.5 nm gate. It would appear that SERG should not be an issue for deep sub-micron CMOS circuits.

Radiation induced single event latch-up (SEL) occurs when a highly ionising particle deposits enough charge in a small volume of the silicon substrate to switch on a parasitic thyristor which causes a very high current to flow between the power supplies [3]. If this current is not detected quickly and the supplies interrupted the chip may be destroyed. The effect occurs above a critical threshold for the charge deposition defined by the Linear Energy Transfer (LET). One way of avoiding SEL is to use guard rings and substrate contacts extensively throughout a design. Fortunately, the design techniques which are used to limit the total dose effects also include the extensive use of guard rings. The 0.25 μm process which will be used for many of the LHC components has been tested to an LET of 89 MeV cm^2 mg^{-1} and no SEL was detected [7].

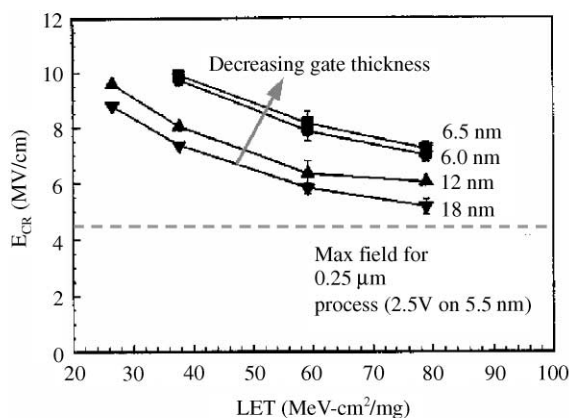

Fig. 2. The measured critical electric field for SERG for different oxide thicknesses taken from Ref. [5]. As the oxide thickness decreases, the critical field for SEGR increases. Also shown in the plot is the maximum permitted field in a 0.25 μm process.

Radiation induced single event upset (SEU) occurs when a highly ionising particle deposits charge near a low capacitance node causing the logical level of the node to switch state. As for SEL, there is a threshold LET above which this effect may occur. The threshold LET tends to decrease with CMOS scaling and is a real concern for deep sub-micron circuits. In general, dynamic nodes are much more sensitive than static nodes and therefore, dynamic logic should be avoided in a high radiation environment. Static logic can be made almost SEL resistant by adding redundancy such that when one node is upset, there are two others which out-vote it in deciding which is the correct state. An example of such a circuit is discussed in Ref. [8].

In summary, deep sub-micron CMOS can be rendered radiation tolerant to Mrad levels by using special layout and circuit configurations. The limitations of such an approach will be explained in what follows citing some typical examples.

4. Circuit design implications for present day radiation tolerant CMOS

As explained earlier, NMOS gates must be closed to avoid leakage paths from drain to source. Unfortunately, this implies that precise NMOS current mirrors are difficult to design as W/L ratios are inherently large [5]. However, circuit structures such as the one shown in Fig. 3 can be used to overcome this limitation at the expense of circuit complexity.

Furthermore, the use of redundant nodes in logic to avoid SEU also increases circuit complexity. However, rather complicated chips have been

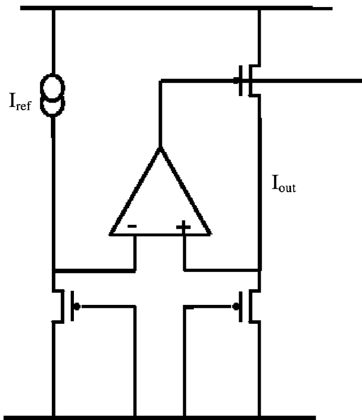

Fig. 3. An example of how to mirror a current avoiding large NMOS devices.

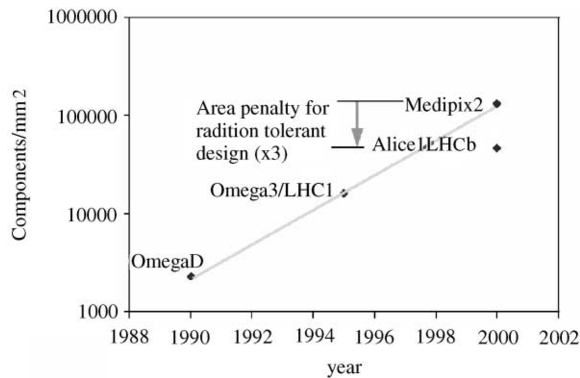

Fig. 4. Component density versus time for silicon detector readout electronics.

designed successfully using such techniques. A good example is the Alice1LHCb pixel readout chip [9,10] which followed on from a prototype chip [11] developed in the same 0.25 μm technology. Results from the prototype chip indicated radiation hardness exceeding 30 Mrad (SiO_2). To illustrate the effect of these layout techniques on circuit density, Fig. 4 shows the component density achieved using different pixel readout chips as an illustration. The chips, OmegaD [12], Omega3/LHC1 [13] and Medipix2 [14], were designed without the use of the special layout and circuit techniques. The Alice1LHCb chip uses these techniques and suffers an area penalty of about a factor 3 compared with Medipix2. Both chips use the same 0.25 μm technology.

5. Challenges and benefits of future scaling

While it may be true that most of the electronic components used in the first versions of the LHC inner detectors will be in 0.25 μm technology, the semiconductor industry will continue its relentless march to smaller and smaller devices. This provides new opportunities and challenges to physicists and circuit designers.

One considerable challenge to circuit designers is that the maximum permitted power supply voltage is shrinking faster than the transistor threshold voltage. A proportional decrease of the transistor threshold voltage with the power supply is prohibited by the constant weak inversion slope of the transistor [15] which would result in a high off leakage current. In design terms, this implies that the voltage excursions on intermediate nodes should be kept to a minimum and that few transistors be used in one branch. At the level of the individual transistor, the range of voltages over which it follows the square law is gradually reduced for smaller gate lengths [16]. Many present day circuit configurations will become obsolete and current mode circuits will have to be developed with all the inherent challenges of optimising speed/noise/power. For circuits requiring high dynamic range, oversampling techniques may have to be considered.

Device threshold voltage matching is governed by the expression

$$\sigma(V_t) = \frac{A_v}{\sqrt{WL}} \quad (1)$$

where V_t is the transistor threshold voltage, A_v a constant for a given technology and W and L are, respectively, the transistor width and length. A rough guide was given [17] which says that in a well controlled technology A_v should be lower than 1 mV μm per nm of gate oxide thickness. Therefore, as the gate dimensions decrease, the device matching improves for a constant device

area. In circuits, such as those used for pixel detector readout, this effect can lead to improved performance or reduced circuit (and therefore cell) size.

Other challenges remain. Dedicated digital libraries have to be developed and maintained for radiation tolerant readout chips. These will have to be regenerated every time the technology is changed. Moreover, new technologies will have to be verified for radiation effects. In particular, IC manufacturers may find it necessary to change the material used for the transistor gate isolation. This could have serious implications for radiation tolerance. Increasingly expensive CAE tools are required to thoroughly verify designs before submission. This becomes even more important as the cost of accessing deep sub-micron technologies is also rising steeply with time.

There are non-negligible problems at the management level as well. Strong design teams have to be kept within the HEP community to guarantee efficient use of the new processes. Maintaining such skills in an exponentially growing marketplace is difficult. Some work can be outsourced but radiation hard electronics is of little commercial interest. The HEP community has to learn from past experience to avoid over-conservative technology choices which fall victim to process obsolescence caused by the economics of a fast moving industry.

6. Conclusions

Present day deep sub-micron CMOS technologies have proven to be radiation hard and suitable for applications at the LHC. Microelectronics is a key enabling technology for particle tracking applications. For macro-economic reasons, it is essential that the HEP community follows the industry trends and tries to adapt the latest technologies to its needs. Strong teams of experts and a reasonable infrastructure are required if the HEP community is to be able to follow the trends. The further scaling of CMOS technologies offers many challenges and opportunities for future tracking systems.

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